深圳市勋瑞光电科技有限公司

Xunrui Shenzhen Optoelectronics Technology Co., Ltd.

CERT. No. QAC0946535 (ISO9001)

CERT. No. HKG002005 (ISO14001)

Product Specification

Customer: _____

Model Name: H0236PHV40E2006

Date: _____

Version: _____

■ **Preliminary Specification**

☐ **Final Specification**

For Customer's Acceptance

Approved by	Comment

Approved by	Reviewed by	Prepared by

Contents

1.Record of Revision

Rev	Issued Date	Description	Editor
1.0	2012/02/15	First Release.	Rich Liang

2 General Specifications

Feature		Spec
Characteristics	Size	2.36inch
	Resolution	480(horizontal)*234(Vertical)
	Interface	8 bit serial (RGB)data input form controller/Raw data/ccir656,601
	Connect type	Connector
	Color	16.7M Color
	Technology type	a-Si
	Display Spec. Pixel pitch (mm)	0.3 x 0.1525
	Pixel Configuration	Delta RGB type
	Display Mode	Normally white TN
	Driver IC	OTA5182A
	Surface Treatment	3H
	Viewing Direction	6 o'clock
Mechanical	LCM (W x H x D) (mm)	55.2*47.55*2.75
	Active Area(mm)	48*35.685
	With /Without TSP	Without TSP
	Weight (g)	TBD
	LED Numbers	2 LEDs

Note 1: Viewing direction is follow the data which measured by optics equipment.
Note 2: Requirements on Environmental Protection: RoHS
Note 3: LCM weight tolerance: +/- 5%

3 Input/Output Terminals

PIN NO.	PIN NAME	DESCRIPTION
1	VCOM	Power supply pad for the TFT- display counter electrode.
2	NC	--
3	VGL	power supply for gate off voltage Connect this pad with a stabilizing capacitor.
4	C4P	Pins to connect capacitance for power circuitry
5	C4N	Pins to connect capacitance for power circuitry
6	VGH	power supply for gate on voltage Connect this pad with a stabilizing capacitor.
7	FRP	--
8	VCAC	Connect this pad with a stabilizing capacitor.
9	VDD_25V	Connect this pad with a stabilizing capacitor.
10	C3P	Pins to connect capacitance for power circuitry
11	C3N	Pins to connect capacitance for power circuitry
12	VDD3	Connect this pad with a stabilizing capacitor.
13	C2P	Pins to connect capacitance for power circuitry
14	C2N	Pins to connect capacitance for power circuitry
15	VDDA	Generated power output pad for source driver block Connect this pad with a stabilizing capacitor.
16	C1P	Pins to connect capacitance for power circuitry
17	C1N	Pins to connect capacitance for power circuitry
18	GND	Power ground
19	VDD	Power supply for analog circuit blocks (2.4 ~ 3.3 V)

20	DRV	--
21	LEDA	LED backlight anode.
22	NC	--
23	FB (LEDK)	Tearing effect output pin to synchronize MPU to frame writing
24	NC	--
25	AGND	Power ground
26	VDDIO	Power supply for interface logic circuits (1.65 ~ 3.3V)
27	CSB	Chip select input pin (“Low” enable).
28	SDA	Serial data input/output and applied on the rising edge of the SCL signal.
29	SCL	This pin is used serial interface clock.
30	HSYNC	Line synchronizing signal for RGB interface operation.
31	VSYNC	Frame synchronizing signal for RGB interface operation.
32	DCLK	Dot clock signal for RGB interface operation.
33	D7	Data Input: MSB
34	D6	Data Input
35	D5	Data Input
36	D4	Data Input
37	D3	Data Input
38	D2	Data Input
39	D1	Data Input
40	D0	Data Input

The external capacitor is required on those pins as following.

4 Absolute Maximum Ratings

Driving TFT LCD Panel

Item	Symbol	MIN	MAX	Unit	Remark
Supply Voltage	V_{CC}	-0.3	4.6	V	
Input Voltage	IOVCC	-0.3	5.0	V	
Operating Temperature	T_{OPR}	-20	70	℃	
Storage Temperature	T_{STG}	-30	80	℃	

5 Electrical Characteristics

5.1 Driving TFT LCD Panel

Ta = 25 °C

Item		Symbol	MIN	TYP	MAX	Unit	Remark
Digital Supply Voltage		V_{CC}	3.0	-	3.6	V	
Logic Signal Input /Output Voltage		IOVCC	3.0	-	3.6	V	
Input Signal Voltage	Low Leve	V_{IL}	VSS	-	0.2x IOVCC	V	
	High Level	V_{IH}	0.8x IOVCC	-	IOVCC	V	
TFT Common Electrode		V_{COMH}	4.5	-	5	V	
TFT Gata ON Voltage		V_{GH}	16.5	-	20	V	
TFT Gata ON Voltage		V_{GL}	-7	-	-5.5	V	

5.2 Driving Backlight

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	I_F	-	30		mA	
Forward Voltage	V_F	3	3.2		V	
Backlight Power consumption	W_{BL}	-	TBD	-	W	

Note 1: Each LED : IF =15 mA, VF =3.2V.
Note 2: Optical performance should be evaluated at Ta=25℃ only.
Note 3: If LED is driven by high current, high ambient temperature & humidity condition. The life time of LED will be reduced.Operating life means brightness goes down to 50% initial brightness. Typical operating life time is estimated data.

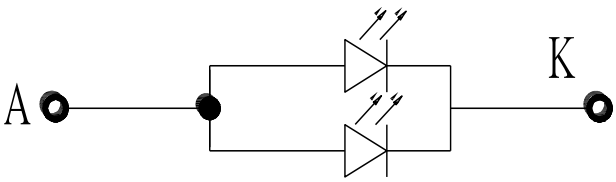
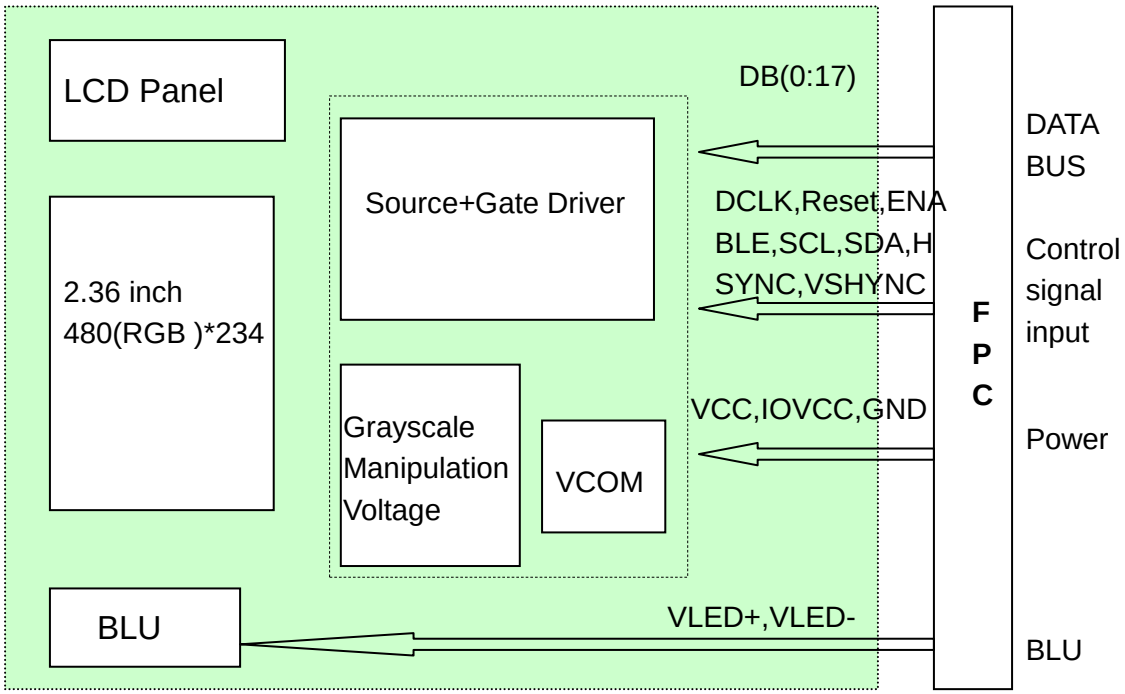


Figure : LED connection of backlight

5.3 Block Diagram



6 Interface Timing

6.1. Absolute maximum ratings

Table 2: Absolute maximum ratings

Parameter	Symbol	Unit	Rating	Note
Logic supply	VDDIO	V	-0.5 to +6	
Analog supply	VDDA	V	-0.5 to +6	
Power supply	VDD	V	-0.5 to +6	
Input Voltage	Others	V	-0.3 to VDDIO+0.3	
Output Voltage	S1~ S480	V	-0.3 to VDDA+0.3	
	Others	V	-0.3 to VDDIO+0.3	
Operating Temperature	T_{OPR}	°C	-30 to +85	
Storage Temperature	T_{STG}	°C	-55 to +100	

Note: If Ics are stressed beyond those listed above "absolute maximum ratings", they may be permanently destroyed. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

6.2. Digital DC characteristics

Table 3: Digital DC characteristics (VDD=3.3V, AGND=GND=0V, T_{OPR} = -30°C to +85°C

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply Voltage	VDDIO		1.8	3.3	3.6	V
Low Level Input Voltage	Vil	Digital input pins	GND	-	0.3xVDDIO	V
High Level Input Voltage	Vih	Digital input pins	0.7xVDDIO	-	VDDIO	V
High Level Output Voltage	Voh	Q1H: Ioh = 400μA	VDDIO-0.4	-	VDDIO	V
Low Level Output Voltage	Vol	Q1H: Iol = -400μA	GND	-	GND+0.4	V
Input Leakage Current	Iil		-	-	±1.0	μA
Digital Stand-by Current	Ist	DCLK is stopped, Outputs are High-Z	-	-	100	μA
Digital Operating Current	Icc	Fclk=24.54 MHz, Fld=15KHz	-	5	7.5	mA

6.3. Analog DC characteristics

Table 4: Analog DC characteristics (VDDIO=3.3V, VDD=3.3V, AGND=GND=0V, T_{OPR} = -30°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply Voltage	VDDA		5	5.7	6.5	V
Voltage Deviation of Outputs	Vvd	Sn=0.2V~0.5V, Sn=4.8V~4.5V	-	±20	±35	mV
		Sn = 0.5V ~ 4.5V	-	±15	±20	
Dynamic Range of Output	Vdr	S1 ~ S480	0.2	-	4.8	V
Analog Stand-by Current	Ist	STB="0"	-	-	100	μA
Analog Operating Current	IDD	No load, line inversion, DCLK=27MHz, Th=63.5us	-	2.0	2.8	mA

6.4. Power DC characteristics

Table 5: Analog DC characteristics (VDDIO=3.3V, VDD=3.3V, AGND=GND=0V, T_{OPR} = -30°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply Voltage	VDD		3.0	3.3	3.6	V
DRV output voltage	VDRV		0	-	VDD	V
Feed back voltage	VFB	DC/DC operating, VBL current=20mA DC_FB_LEVEL=100	0.55	0.6	0.65	V
Base drive current	IDRV	VDDIO=3 V,DRV=0.7 V	-	-	10	mA
VCOM AC voltage	$VCOM_{AC}$	Function of VCOM_AC[3..0] setting	4.5	5.0	5.2	V
Low level Output current	IOL_{FRP}	Sink current Vo=0.5V		-10	-	mA
High level Output current	IOH_{FRP}	Driving current Vo=VCAC-0.5V		-10	-	mA
Positive high-voltage power	VGH	No Load	16.5	18.5	20	V
Negative high-voltage power	VGL	No Load; function of VCOM_AC[3..0] setting.	-7	-6	-5.5	V
Power Stand-by Current	Ipst	STB="0"	-	-	100	μA
Power Operating Current	IPDD	DCLK=27MHz, Th=63.5us	-	12	14	mA

6.5. AC characteristics

Table 6: AC characteristics (VDD=3.3V, AGND=GND=0V, T_{OPR} = -30°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CLK pulse duty	Tcw		40	50	60	%
Delay between Hsync and DCLK	Thc		-	-	1.0	DCLK
Hsync width	Twh		1.0	-	-	DCLK
Hsync period	Th		60	63.56	67	us
Vsync setup time	Tvst		12	-	-	ns
Vsync hold time	Tvhd		12	-	-	ns
Hsync setup time	Thst		12	-	-	ns
Hsync hold time	Thhd		12	-	-	ns
Data set-up time	Tdsu	D00~D07 to DCLK	12	-	-	ns
Data hold time	Tdhd	D00~D07 to DCLK	12	-	-	ns
VSync to 1st gate Output	Tstv	Sel="111";By HDL[3..0] settings	6	13	21	Th
CCIR V to 1st gate Output	Tstv	Sel="111" NTCS (PAL=0); By HDL[3..0] settings	14	21	29	Th
CCIR V to 1st gate Output	Tstv	Sel="111" PAL=1; By HDL[3..0] settings	20	27	35	Th
SD output stable time	Tst	30mV precision; CL=6.75pF, R=3.62K	-	25	30	us
GD output delay time	Tgd	CL=17.6pF, R=1.29K	-	900	1500	ns
GD output rise and fall time	Tgst	CL=17.6pF, R=1.29K 10% to 90%	-	900	1500	ns
Serial communication						
Serial clock period	Tsck		320	-	-	ns
Serial clock duty cycle	Tscw		40	50	60	%

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Serial clock width low/high	Tssw		120			ns
Serial data setup time	Tist		120			ns
Serial data hold time	Tihd		120			ns
CSB setup time	Tcst		240			ns
CSB data hold time	Tchd		120			ns
Chip select distinguish	Tcd		1			us
Delay between CSB and Vsync	Tcv		1			us

6.3 SPI FORMAT

There is a total of 16 registers each containing several parameters. For a detailed description of the parameters refer to Table 1.

The serial register has read/write function. D[15:12] are the register address, D[11] defined the read or write mode and D[10:0] are the data.

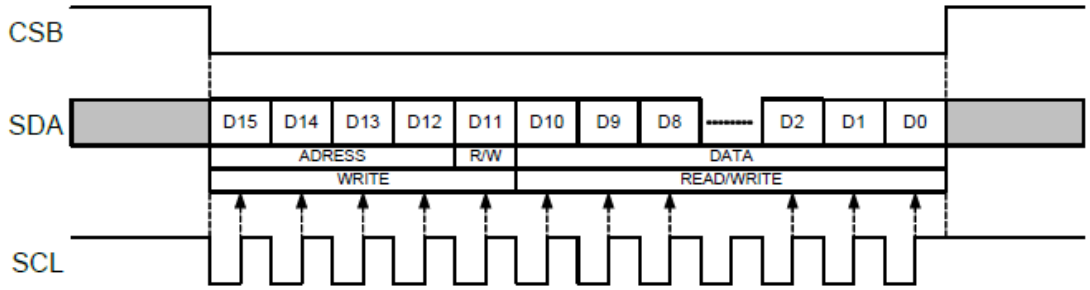


Figure 2: Serial Interface read/write sequence

At power-on, the default values specified for each parameter (in Table 1) are taken.

All data, except S0 D[3:2], are validated on the negative edge of Vsync.

In 3-wire register, GRB clear registers to default value except GRB value.

If less than 16-bit data are read during the CS low time period the data is cancelled.

6.4 Power ON/OFF Sequence

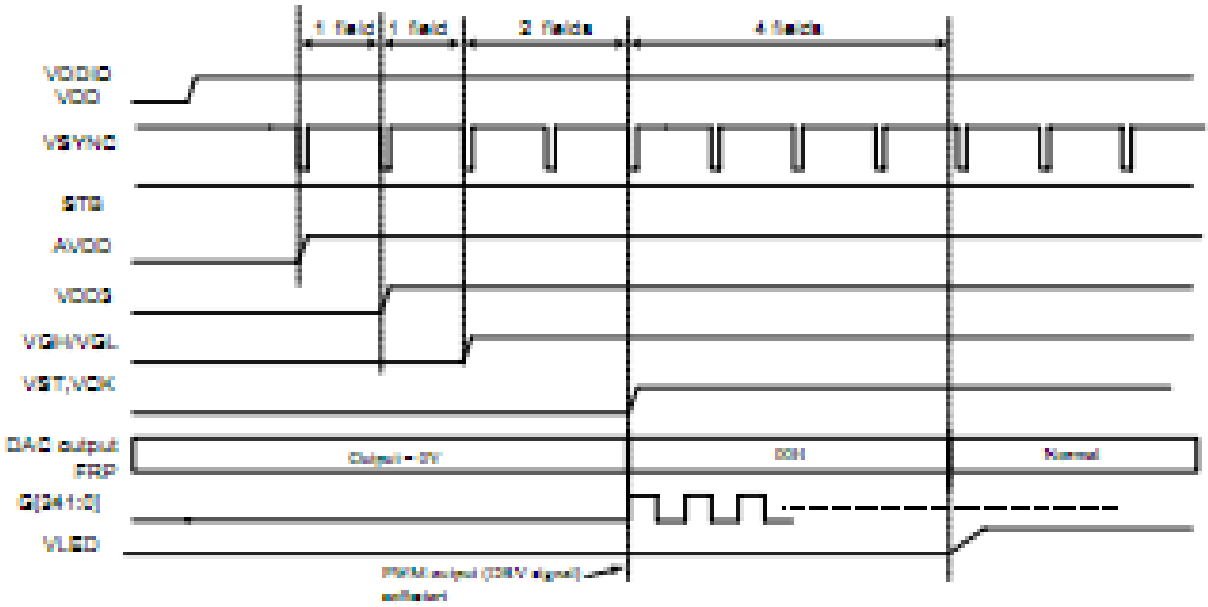


Figure 3: Power on sequence

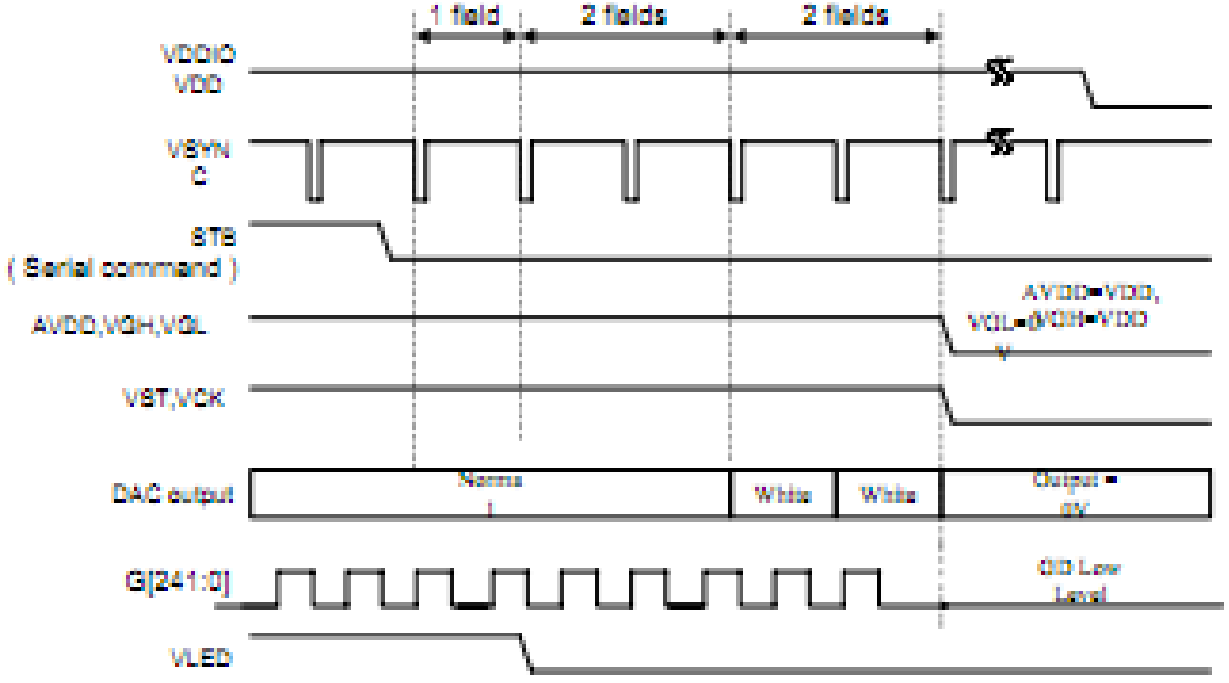
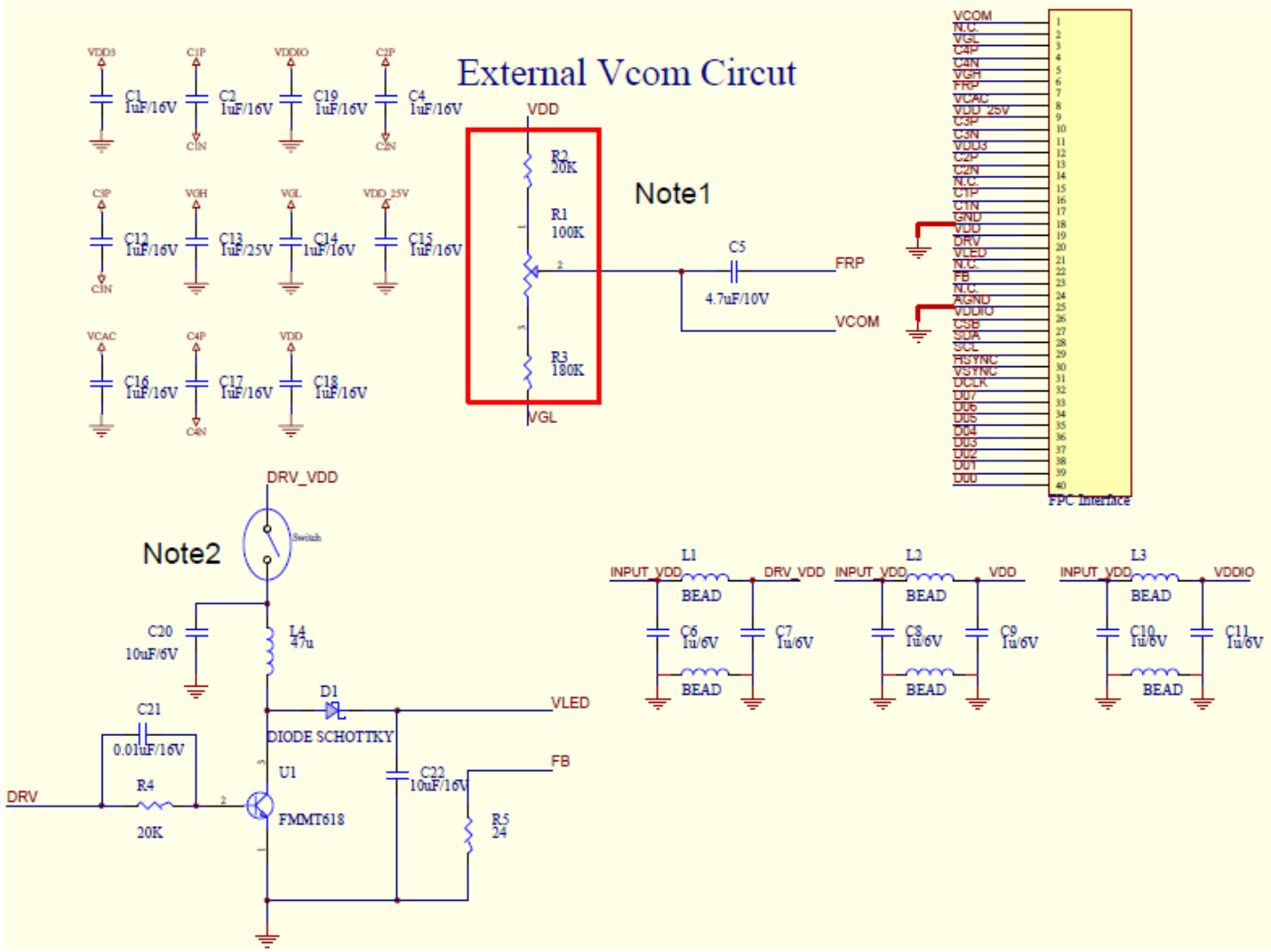


Figure 4: Power off sequence

6.5 Reference application note



6.6. Operating mode dependent AC characteristics

6.6.1. RAW DATA MODE

The below specifications apply for:

SEL2	SEL1	SEL0
0	0	0

Table 7: RAW DATA MODE 480x240 AC characteristics (VDD=3.3V, AGND=GND=0V, T_{OPR} = -30°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DCLK frequency	Fclk		-	9.7	-	MHz
DCLK period	Tcph		-	103	-	ns
Delay from Hsync to Source Output	Thso		-	56	-	DCLK
Delay from Hsync to Gate Output	Thgo		-	45	-	DCLK
Delay from Hsync to Gate Output off	Thgz		-	19	-	DCLK
Delay from Hsync to 1st data input	Ths	Function of DDL[4..0] settings	84	100	115	DCLK
DC converter osc. Frequency	Fosc	Fclk/32	-	303.1	-	kHz

6.6.2. SERIAL RGB MODE

The below specifications apply for:

SEL2	SEL1	SEL0
0	0	1

Table 8: SERIAL MODE, AC characteristics (VDD=3.3V, AGND=GND=0V, T_{OPR} = -30°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DCLK frequency	Fclk		-	24.54/27	-	MHz
DCLK cycle time	Tcph		-	40/37	-	ns
Delay from Hsync to Source Output	Thso		-	143	-	DCLK
Delay from Hsync to Gate Output	Thgo		-	113	-	DCLK
Delay from Hsync to Gate Output off	Thgz		-	48	-	DCLK
Delay from Hsync to 1st data input	Ths	Function of DDL[4..0] settings	236	252	267	DCLK
DC converter osc. Frequency	Fosc	Fclk/64 = 383.4kHz / 421.9kHz	-	383.4 / 421.9	-	kHz

6.6.3. CCIR

The below specifications apply for:

SEL2	SEL1	SEL0
1	1	1

Table 9:CCIR MODE, AC characteristics (VDD=3.3V, AGND=GND=0V, T_{OPR} = -30°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DCLK frequency	Fclk		-	27	-	MHz
DCLK cycle time	Tcph		-	37	-	ns
CLK pulse duty	Tcw		40	50	60	%
Delay from EAV to Source Output	Thso		-	143	-	DCLK
Delay from EAV to Gate Output	Thgo		-	113	-	DCLK
Delay from EAV to Gate Output off	Thgz		-	48	-	DCLK
Delay from EAV to 1st data input	Ths	Function of DDL[4..0] settings	257	273	288	DCLK
DC converter osc. Frequency	Fosc	Fclk/64	-	421.9	-	kHz

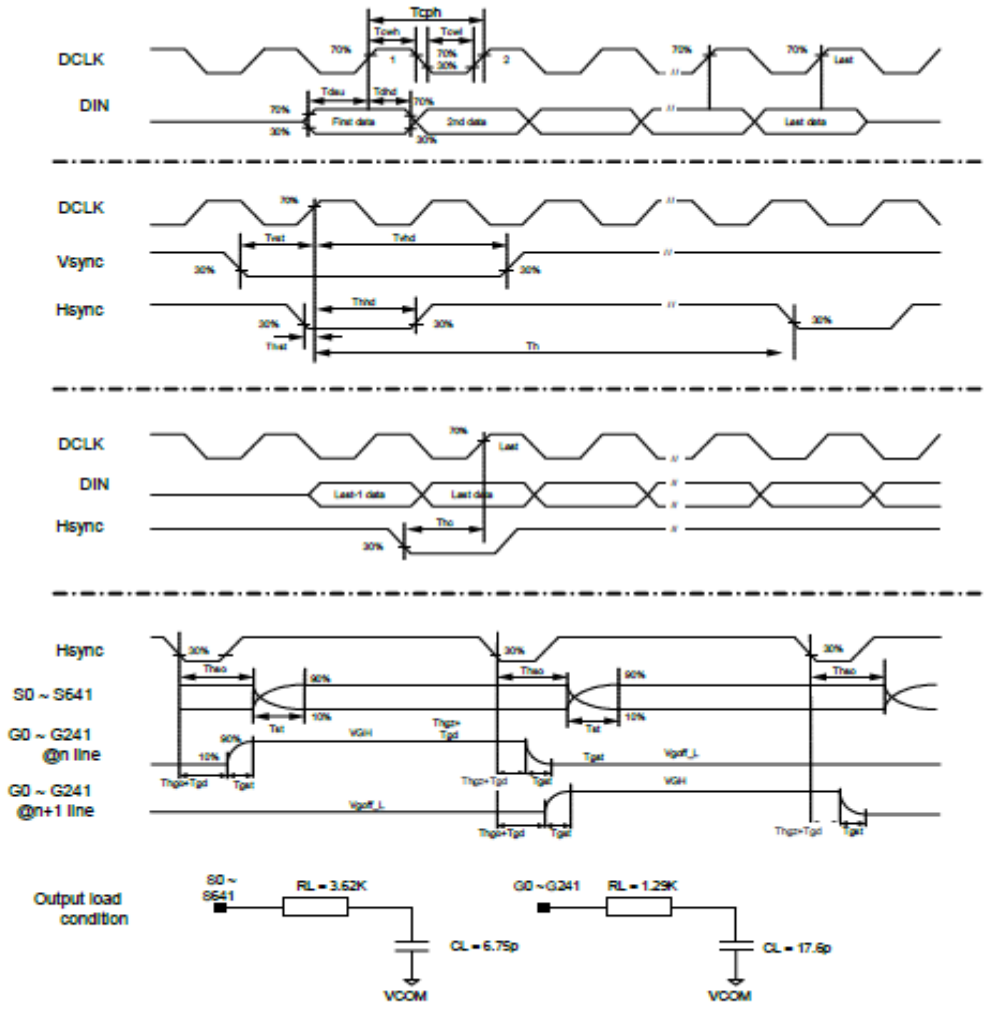


Figure 5: AC Drivers timing

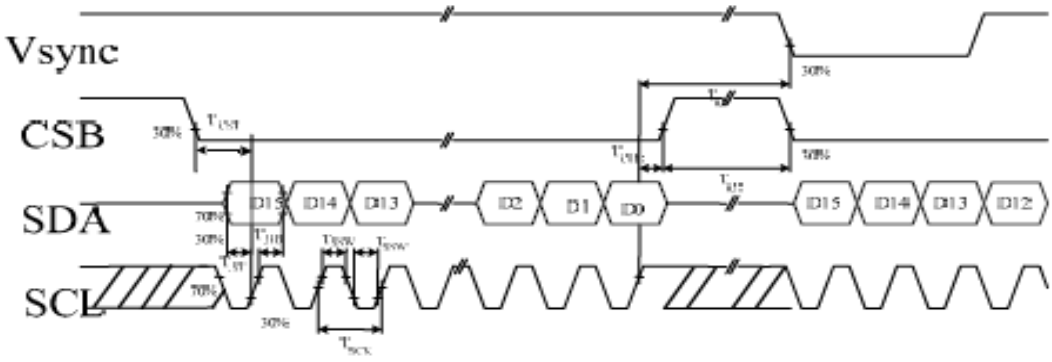
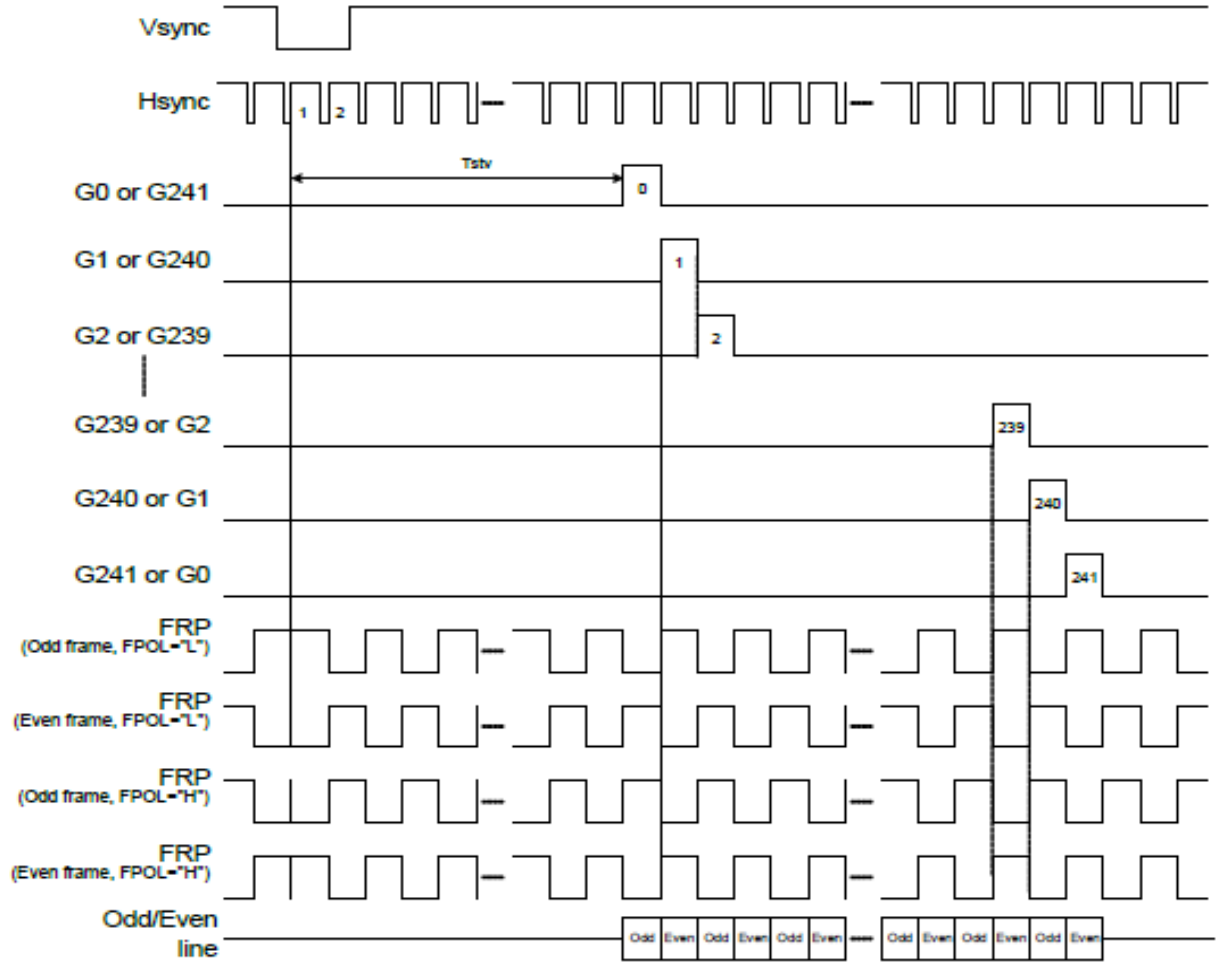


Figure 6: AC Serial communication timing



Note: SD Line 1,3,5,..., 241 =Odd line, : SD Line 2,5, 6,..., 242 =Even line

Figure 7: Vertical timing diagram

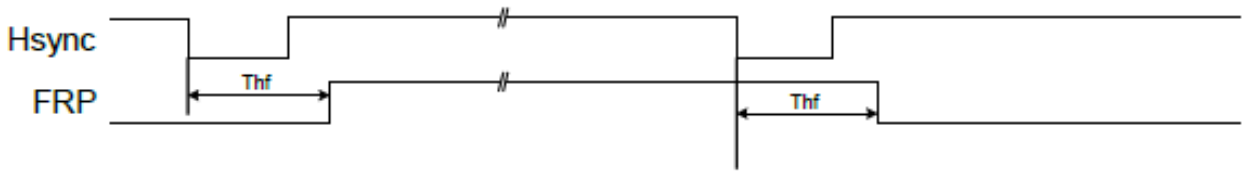


Figure 8: Horizontal timing diagram

6.7. Input Data Format

6.7.1. RAW DATA MODE

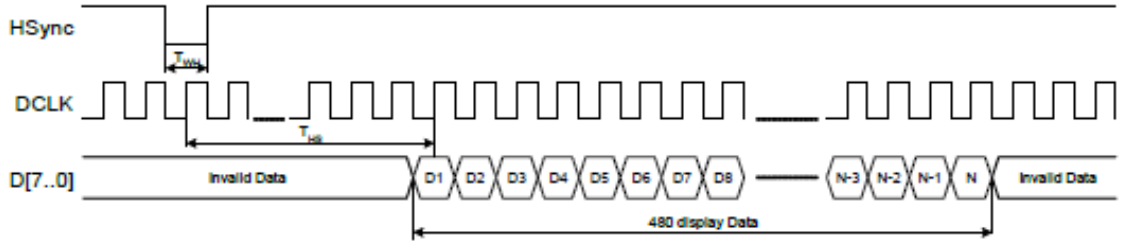


Figure 9: RAW DATA MODE data input format

6.7.2. SERIAL MODE 24.54MHz

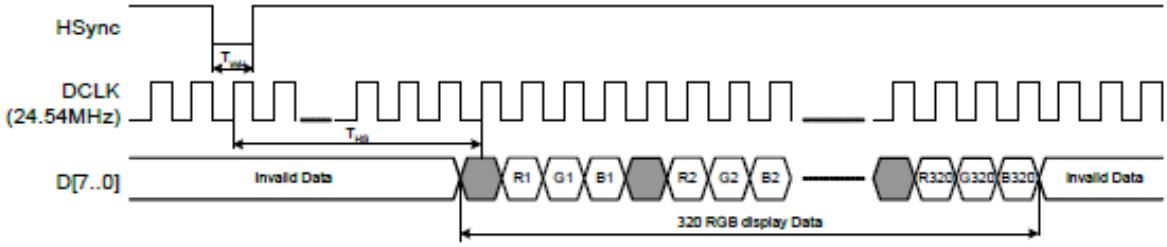


Figure 10: SERIAL MODE 24.54MHz Data input format (Sel=001)

6.7.3. SERIAL MODE 27MHz

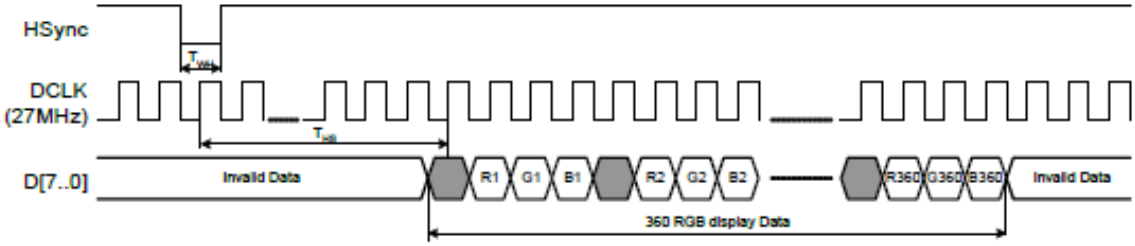


Figure 11: SERIAL MODE 27MHz Data input format (Sel=010)

6.8. Vertical input timing

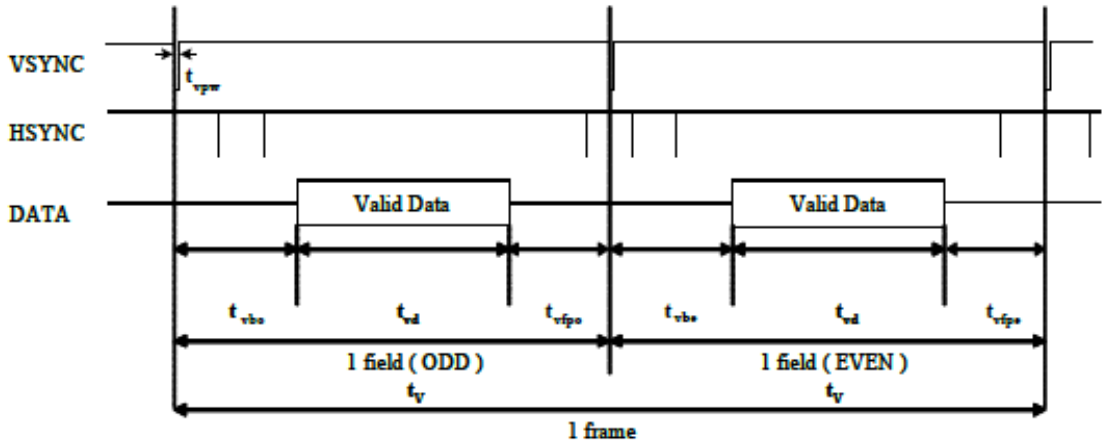


Figure 13: Vertical input timing diagram for interlace application

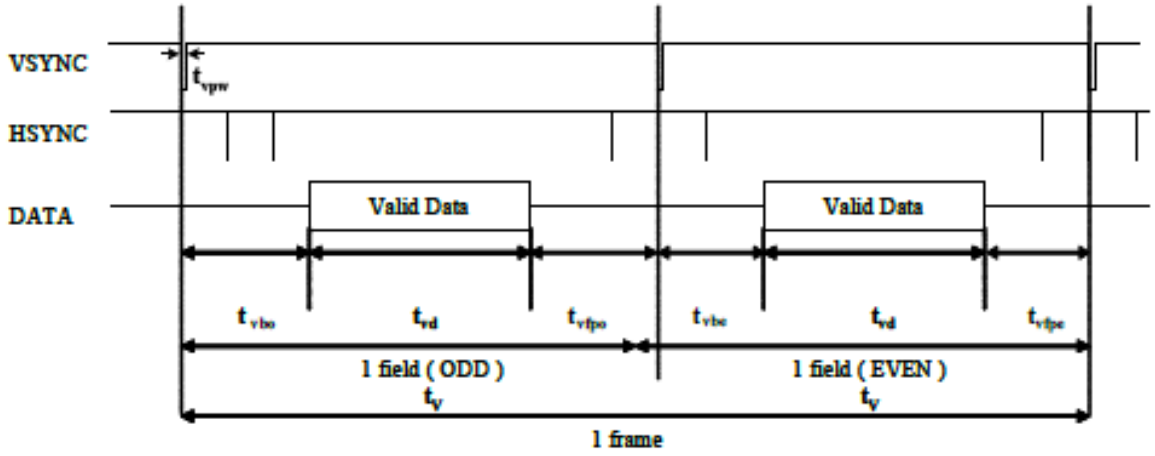


Figure 14: Vertical input timing diagram for non-interlace application

6.8.1. Raw data vertical input timing

Parameter		Symbol	Interlace			(*)Non-Interlace			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Vertical display area		t_{vd}		240			240		H
VSYNC period time		t_v	247.5	262.5	277.5	247	262	277	H
VSYNC pulse width		t_{vpw}	1 DCLK	1H	6H	1 DCLK	1H	6H	
(*)VSYNC Blanking (t_{vb})	Odd field	t_{vbo}	6	13	21	6	13	21	H
	Even field	t_{vbe}	6.5	13.5	21.5				
VSYNC Front porch (t_{vfp})	Odd field	t_{vfpo}	1.5	9.5	16.5	1	9	16	H
	Even field	t_{vfpe}	1	9	16				

6.8.2. SERIAL RGB vertical input timing

NTSC

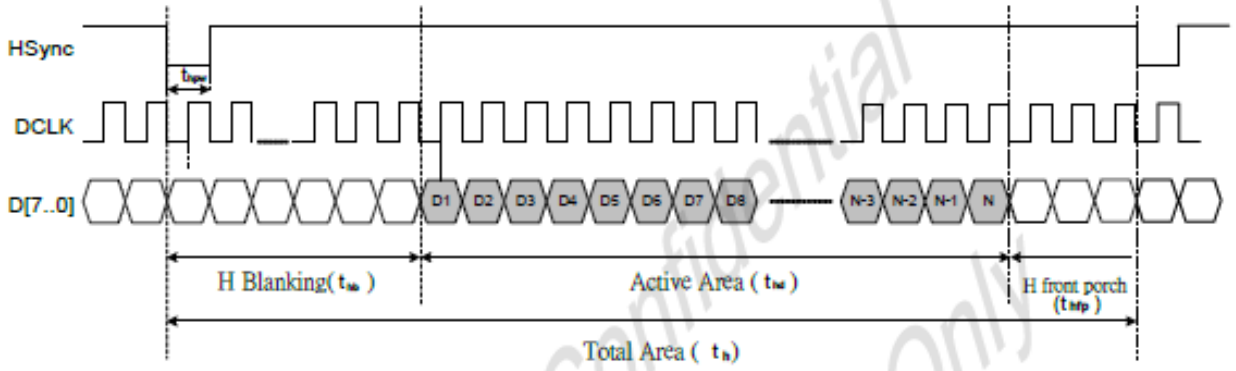
Parameter		Symbol	Interlace			(*)Non-Interlace			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Vertical display area		t_{vd}		240			240		H
VSYNC period time		t_v	247.5	262.5	277.5	247	262	277	H
VSYNC pulse width		t_{vpw}	1 DCLK	1H	6H	1 DCLK	1H	6H	
(*)VSYNC Blanking (t_{vb})	Odd field	t_{vbo}	6	13	21	6	13	21	H
	Even field	t_{vbe}	6.5	13.5	21.5				
VSYNC Front porch (t_{vfp})	Odd field	t_{vfpo}	1.5	9.5	16.5	1	9	16	H
	Even field	t_{vfpe}	1	9	16				

PAL

Parameter		Symbol	Interlace			(*)Non-Interlace			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Vertical display area		t_{vd}		288(280)			288(280)		H
VSYNC period time		t_v	295.5 (287.5)	312.5	325.5 (317.5)	295 (287)	312	325 (317)	H
VSYNC pulse width		t_{vpw}	1 DCLK	1H	6H	1 DCLK	1H	6H	
(*)VSYNC Blanking (t_{vb})	Odd field	t_{vbo}	6	13	21	6	13	21	H
	Even field	t_{vbe}	6.5	13.5	21.5				
VSYNC Front porch (t_{vfp})	Odd field	t_{vfpo}	1.5	11.5(19.5)	16.5	1	11(19)	16	H
	Even field	t_{vfpe}	1	11(19)	16				

(*) Non-Interlace mode: NTSC is 262 lines (typical), but 263 is tolerant.
PAL is 312 lines (typical), but 313 is tolerant.

6.9. Horizontal input timing



6.9.1. Raw Data

Parameter		Symbol	Value			Unit
Horizontal display area		t_{hd}	480			DCLK
DCLK frequency		f_{clk}	Min.	Typ.	Max	
			8.1	9.7	11.3	Mhz
1 Horizontal Line		t_h	617			DCLK
HSYNC pulse width	Min.	t_{hpw}	1			
	Typ.		1			
	Max.		96			
HSYNC blanking		t_{hb}	84	100	115	
HSYNC front porch		t_{hfp}	53	37	22	

6.9.2. SERIAL RGB MODE

NTSC

Parameter		Symbol	Value			Value			Value			Unit
Horizontal display area		t_{hd}	1280			1408			1440			DCLK
DCLK frequency		f_{clk}	Min.	Typ.	Max	Min.	Typ.	Max	Min.	Typ.	Max	
			20.47	24.54	28.66	22.5	27	31.5	22.5	27	31.5	MHz
1 Horizontal Line		t_h	1560			1716			1716			DCLK
HSYNC pulse width	Min.	t_{hpw}	1			1			1			
	Typ.		1			1			1			
	Max.		96			96			96			
HSYNC blanking		t_{hb}	237	252	268	237	252	268	237	252	268	
HSYNC front porch		t_{hfp}	43	28	12	71	56	40	39	24	8	

PAL

Parameter		Symbol	Value			Value			Unit
Horizontal display area		t_{hd}	1408			1440			DCLK
DCLK frequency		f_{clk}	Min.	Typ.	Max	Min.	Typ.	Max	
			22.5	27	31.5	22.5	27	31.5	MHz
1 Horizontal Line		t_h	1728			1728			DCLK
HSYNC pulse width	Min.	t_{hpw}	1			1			
	Typ.		1			1			
	Max.		96			96			
HSYNC blanking		t_{hb}	237	252	268	237	252	268	
HSYNC front porch		t_{hfp}	83	68	52	51	36	20	

6.9.3. 3. CCIR

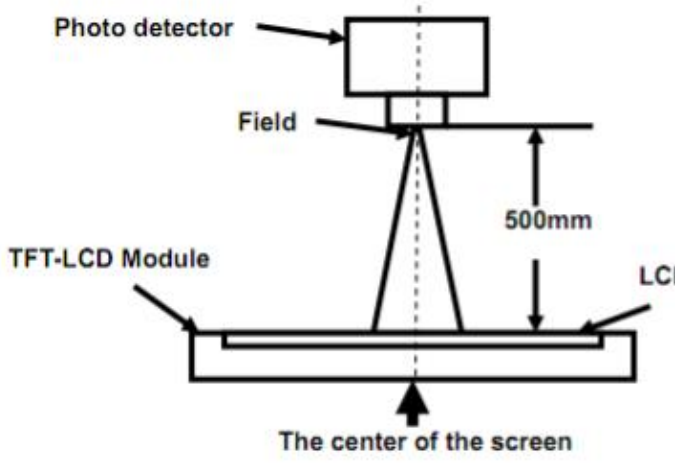
Parameter		Symbol	Mode(NTSC/PAL)	Unit
Horizontal display area		t_{hd}	1440	DCLK
DCLK frequency		f_{clk}	27	MHz
1 Horizontal Line		t_h	1716	DCLK
Internal HSYNC pulse width	Min.	t_{hpw}	1	
	Typ.		1	
	Max.		-	
HSYNC blanking		t_{hb}	268	

7 Optical Characteristics

Items		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing angles		θ_T	Center CR≥10	-	50	-	Degree.	Note2
		θ_B		-	65	-		
		θ_L		-	65	-		
		θ_R		-	65	-		
Contrast Ratio		CR	Θ =0	-	350	-	-	Note1, Note3
Response Time		T_{ON}	25°C	-	20	-	ms	Note1, Note4
		T_{OFF}						
Chromaticity	White	X_W	Backlight power on	0. 282	0.300	0.322	-	Note1, Note5
		Y_W		0.327	0.347	0.367	-	
	Red	X_R		0.593	0.613	0.633	-	
		Y_R		0.311	0.331	0.351	-	
	Green	X_G		0.298	0.318	0.338	-	
		Y_G		0.529	0.549	0.569	-	
	Blue	X_B		0.132	0.152	0.172	-	
		Y_B		0.170	0.190	0.210	-	
Uniformity		U		75	80	-	%	Note1, Note6
Luminance		L		-	200		Nits	Note1, Note7

Test Conditions:
1. IF= 30mA(one channel),the ambient temperature is 25° C.
2. The test systems refer to Note 1 and Note 2.

Note 1:Definition of optical measurement system.
The optical characteristics should be measured in dark room. After 5 minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.



Item	Photo detector	Field
Contrast Ratio	BM-7A	1°
Luminance		
Chromaticity		
Lum Uniformity		
Response Time	SR-3A	2°

Note 2: Definition of viewing angle range and measurement system.
viewing angle is measured at the center point of the LCD by CONOSCOPE(ergo-80).

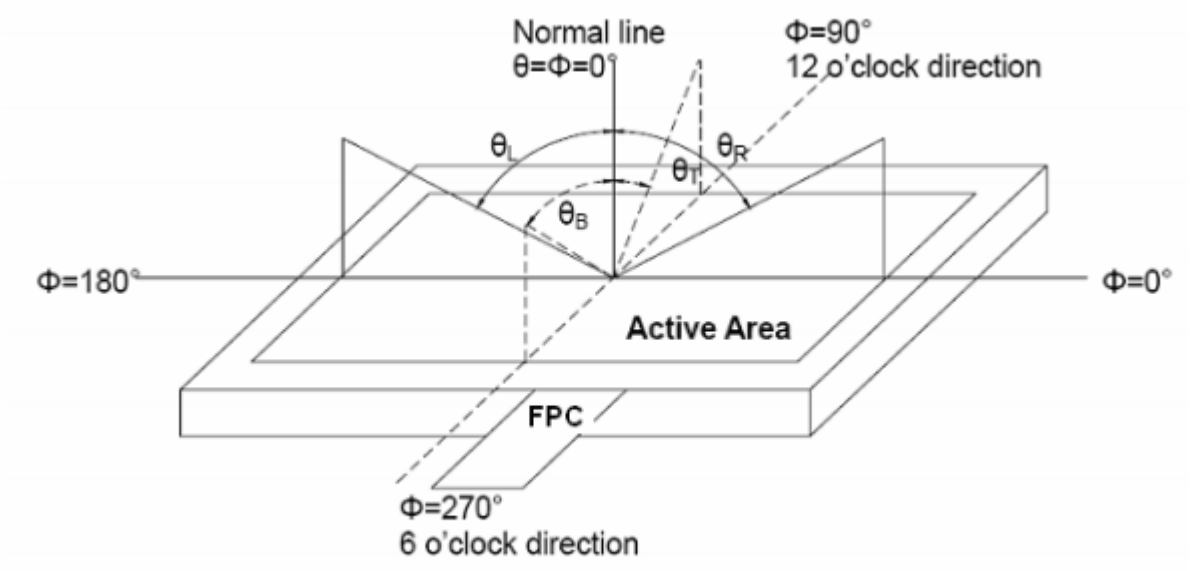


Fig. 1 Definition of viewing angle

Note 3: Definition of contrast ratio

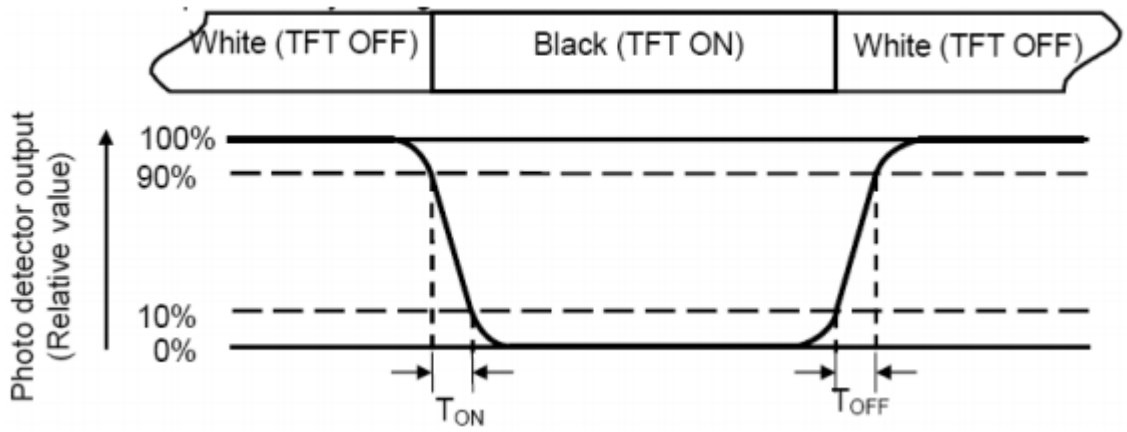
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD is on the "White" state}}{\text{Luminance measured when LCD is on the "Black" state}}$$

“White state “:The state is that the LCD should driven by Vwhite.

“Black state”: The state is that the LCD should driven by Vblack.

Vwhite: To be determined Vblack: To be determined.

Note 4: Definition of Response time
The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time (TON) is the time between photo detector output intensity changed from 90% to 10%. And fall time (TOFF) is the time between photo detector output intensity changed from 10% to 90%.



Note 5: Definition of color chromaticity (CIE1931)
Color coordinates measured at center point of LCD.

Note 6: Definition of Luminance Uniformity
Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity(U) = Lmin/ Lmax X100%

L-------Active area length W----- Active area width

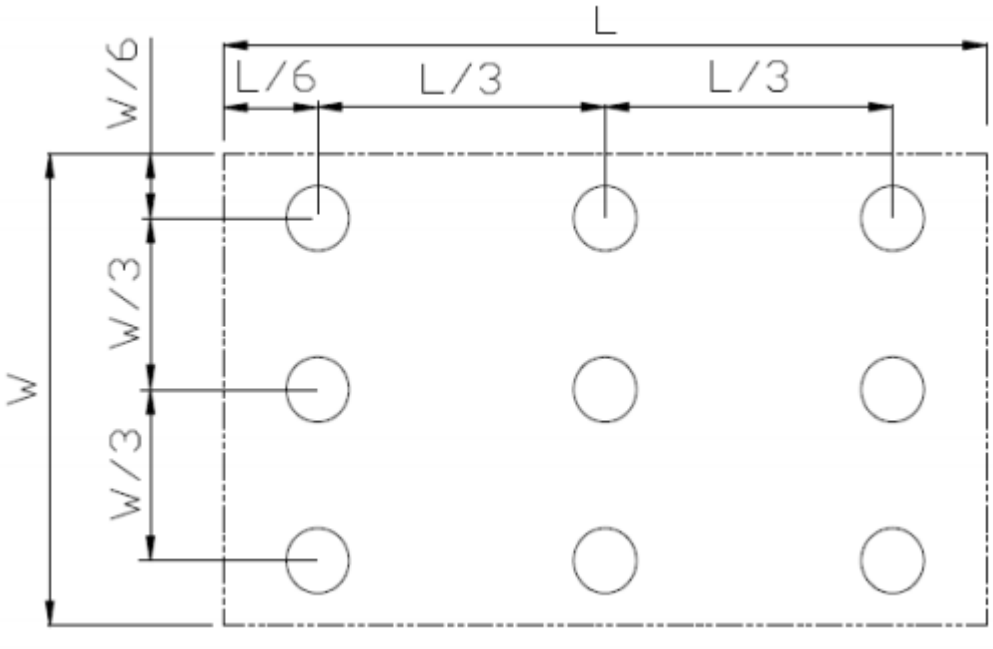


Fig. 2 Definition of uniformity

Lmax: The measured maximum luminance of all measurement position.
Lmin: The measured minimum luminance of all measurement position.

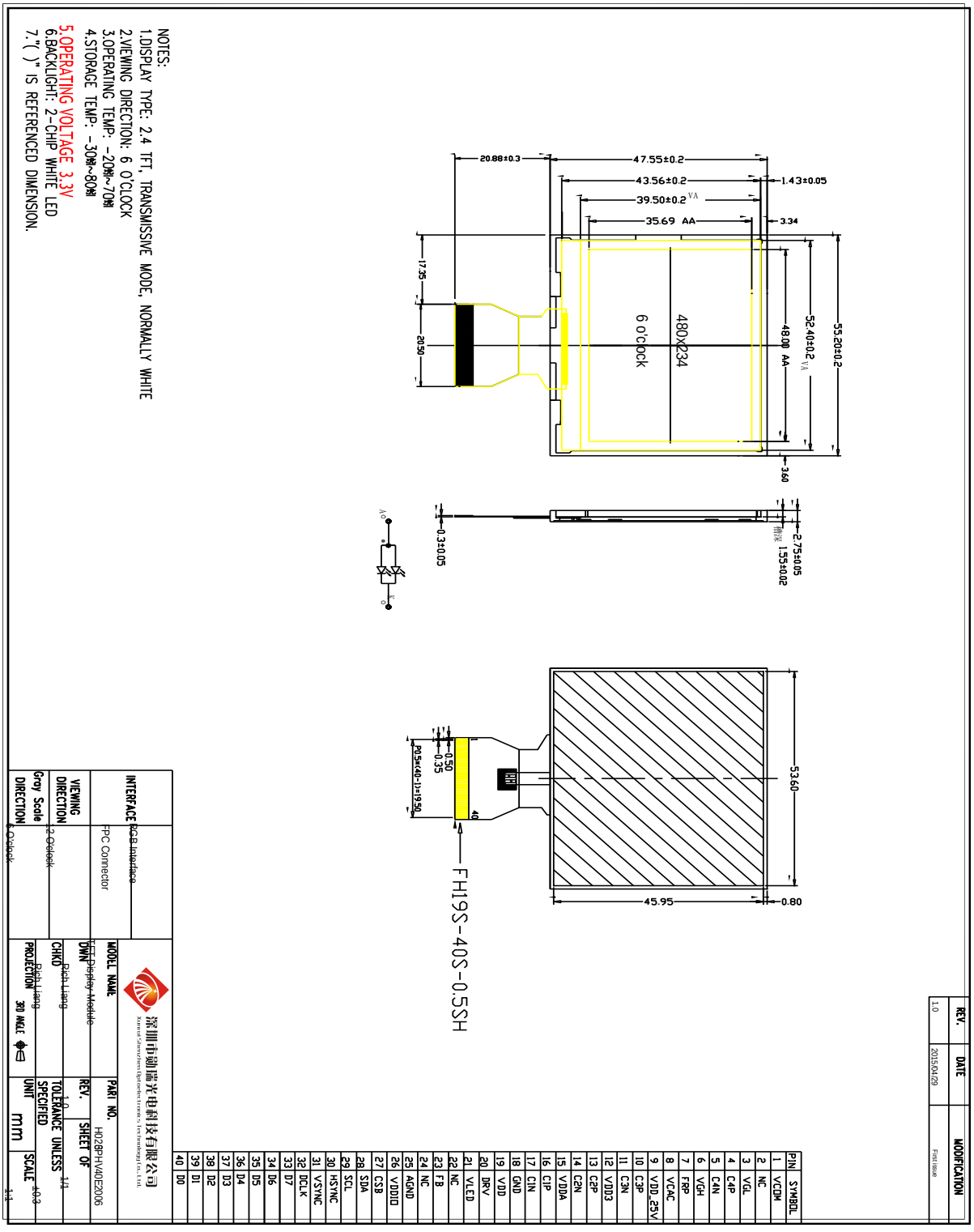
Note 7: Definition of Luminance :
Measure the luminance of white state at center point.

8 Environmental / Reliability Tests

No	Test Item	Condition	Remarks
1	High Temperature Opeartion	Ts= +70℃, 240hrs	Note 1 IEC60068-2-2, GB2423. 2-89
2	Low Temperature Opeartion	Ta= -20℃, 240hrs	Note 2 IEC60068-2-1 GB2423.1-89
3	High Temperature Storage	Ta= +80℃, 240hrs	IEC60068-2-2 GB2423. 2-89
4	Low Temperature Storage	Ta= -30℃, 240hrs	IEC60068-2-1 GB/T2423.1-89
5	High Temperature & Humidity Storage	Ta= +60℃, 90% RH max, 160 hours	IEC60068-2-3 GB/T2423.3-2006
6	Thermal Shock (Non-operation)	-30℃ 30 min ~ +80℃ 30 min Change time: 5min, 30 Cycle	Start with cold temperature,end with high temperature IEC60068-2-14, GB2423.22-87
7	Electro Static Discharge (Opeartion)	C=150pF, R=330 Ω, 5 points/panel Air:±8KV, 5 times; Contact: ±4KV, 5 times; (Environment: 15℃ ~ 35℃, 30% ~ 60%, 86Kpa ~ 106Kpa)	IEC61000-4-2 GB/T17626.2-1998
8	Vibration (Non-operation)	Frequency range: 10~55Hz, Stroke: 1.mm Sweep: 10Hz~55Hz~10Hz 2 hours for each direction of X .Y. Z. (package condition)	IEC60068-2-6 GB/T2423.5-1995
9	Shock (Non-operation)	60G 6ms, ± X, ±Y, ± Z 3 times for each direction	IEC60068-2-27 GB/T2423.5-1995
10	Package Drop Test	Height: 80 cm, 1 corner, 3 edges, 6 surfaces	IEC60068-2-32 GB/T2423.8-1995

Note: 1. T_S is the temperature of panel's surface.
2. Ta is the ambient temperature of sample.

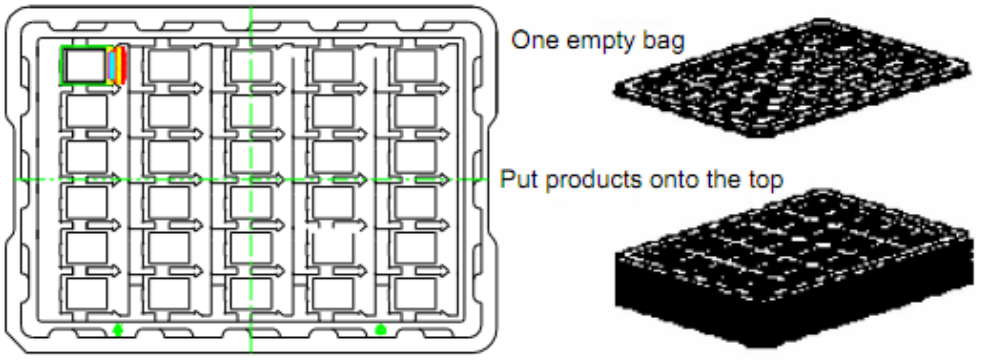
9 Mechanical Drawing


NOTES:
1.DISPLAY TYPE: 2.4 TFT, TRANSMISSIVE MODE, NORMALLY WHITE
2.VIEWING DIRECTION: 6 O'CLOCK
3.OPERATING TEMP: -20℃~70℃
4.STORAGE TEMP: -30℃~80℃
5.OPERATING VOLTAGE 3.3V
6.BACKLIGHT: 2-CHIP WHITE LED
7."( )" IS REFERENCED DIMENSION.
20.88±0.3
47.55±0.2
43.56±0.2
39.50±0.2 VA
35.69 AA
1.43±0.05
3.34
17.35
20.50
6 O'CLOCK
480X234
52.40±0.2 VA
48.00 AA
55.20±0.2
3.60
0.3±0.05
2.75±0.05
1.55±0.02
FH19S-40S-0.5SH
53.60
45.95
0.80
0.50
0.35
0.5x40-1±1950
40
REV.
DATE
MODIFICATION
1.0
2015.04.29
First Issue
PIN SYMBOL
1 VCOM
2 NC
3 VGL
4 C4P
5 C4N
6 VGH
7 FRP
8 VCAC
9 VDD_2.5V
10 C3P
11 C3N
12 VDD3
13 C2P
14 C2N
15 VDDA
16 C1P
17 C1N
18 GND
19 VDD
20 DRV
21 VLED
22 NC
23 FB
24 NC
25 AGND
26 VDDIO
27 CSB
28 SDA
29 SCL
30 HSYNC
31 VSYNC
32 DCLK
33 D7
34 D6
35 D5
36 D4
37 D3
38 D2
39 D1
40 D0
深圳市勋瑞光电科技有限公司
Xunrui Shenzhen Optoelectronics Technology Co., Ltd.
INTERFACE RGB Interface
FPC Connector
MODEL NAME
PART NO. H028PHV40E2006
VIEWING DIRECTION 12 O'clock
DWN Peiqing Meddle
REV. 1.0
CHKD Rich Liang
SHEET OF 1/1
Gray Scale 8 Grade
PROJECTION 3RD ANGLE
TOLERANCE UNLESS SPECIFIED ±0.3
UNIT mm
SCALE 4:1

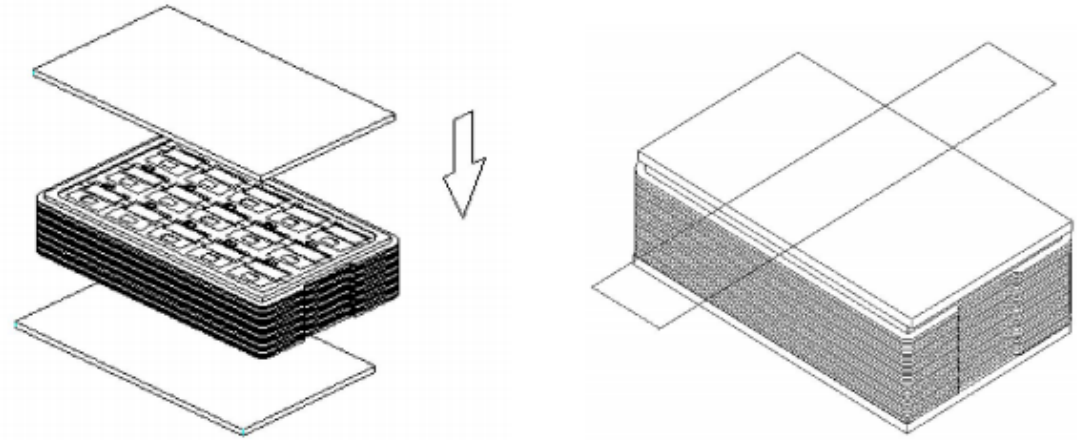
10 Packing

Packing Method

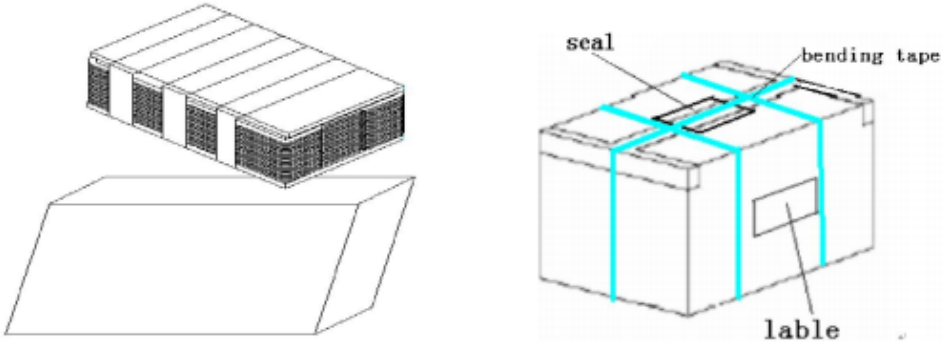
(1) (2)



(3) (4)



(5) (6)



1. Put module into tray cavity:
2. Tray stacking
3. Put 1 cardboard under the tray stack and 1 cardboard above:
4. Fix the cardboard to the tray stack with adhesive tape:
5. Put the tray stack into carton.
6. Carton sealing with adhesive tape.

11 Precautions For Use of LCD modules

11.1 Handling Precautions

11.1.1. The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

11.1.2. If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

11.1.3. Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

11.1.4. The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

11.1.5. If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketone
- Aromatic solvents

11.1.6. Do not attempt to disassemble the LCD Module.

11.1.7. If the logic circuit power is off, do not apply the input signals.

11.1.8. To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

11.1.8.1. Be sure to ground the body when handling the LCD Modules.

11.1.8.2. Tools required for assembly, such as soldering irons, must be properly ground.

11.1.8.3. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

11.1.8.4. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

11.2 Storage Precautions

11.2.1. When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

11.2.2. The LCD modules should be stored under the storage temperature range If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0℃ ～ 40℃ Relatively humidity: ≤80%

11.2.3. The LCD modules should be stored in the room without acid, alkali and harmful gas.

11.3 Transportation Precautions

The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.